MEMS digital output motion sensor

eCompass module with 3D accelerometer and 3D magnetometer

Key Features

- Supply voltage, 2.2V to 3.6V

- 2x2x1.1 mm LGA-12 package
- Digital I^2C output interface
- Low power consumption
- RoHS compliant
- Accelerometer
  - User selectable range, ±2g, ±4g, ±8g, ±16g for accelerometer
  - 14 bit resolution
  - Free-fall detection
  - User selectable data output rate
  - One programmable interrupt generators for motion detection
  - Factory programmable offset and sensitivity
- Magnetometer
  - Full scale:±48Gauss
  - 16-bit resolution
  - Operation mode
    - Power-down mode
    - Burst mode
    - Single measurement mode
    - Wake-up on change mode
    - External trigger measurement mod
  - One programmable interrupt generator for DRDY or Trig function
  - Embedded temperature sensor to compensate sensor temperature effect
  - Embedded self-test to built-in internal magnetic field generator

Applications

- Tilt-compensated compasses
- Map rotation
- Position detection
- Motion-activated functions
- Free-fall detection
- Click/double-click recognition
- Pedometers
- Intelligent power saving for handheld devices
- Display orientation
- Gaming and virtual reality input devices
- Impact recognition and logging

Product Overview

The dc213 is a system-in-package (SiP) featuring a 3D digital linear acceleration sensor and a 3D digital magnetic sensor.

The dc213 has linear acceleration full scales of ±2g / ±4g / ±8g / ±16g and a magnetic field full scale of ±48 gauss.

The dc213 includes an I2C serial bus interface that supports standard and fast mode (100 kHz and 400 kHz) .

The system can be configured to generate an interrupt signal for free-fall, motion detection and magnetic field detection. Thresholds and timing of interrupt generators are programmable by the end user.

Magnetic and accelerometer blocks can be enabled or put into power-down mode separately.

The dc213 is available in a plastic land grid array package (LGA) and is guaranteed to operate over an extended temperature range from -40 °C to +85 °C.

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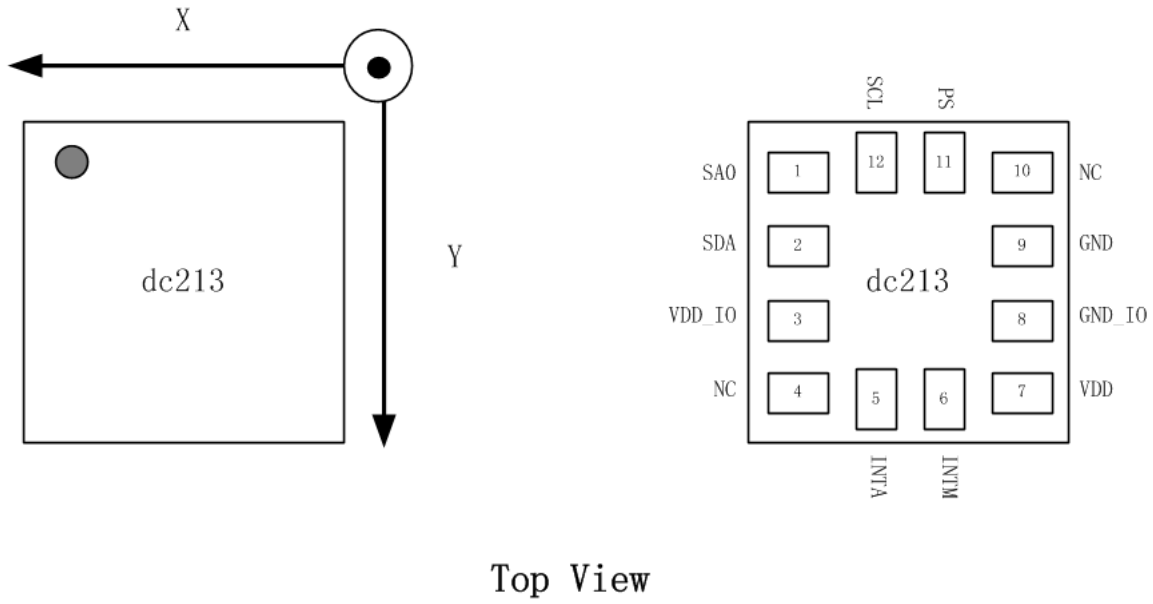


Top View

Figure 1 Pin Description

Table 1.Pin description

Pin#	Name	Function
1	SA0	I2C less significant bit of the accelerometer address (SA0)
2	SDA	I2C serial data input/output(SDA)
3	VDD_IO	Power supply for I/O pins
4	NC	Not connected
5	INTA	Interrupt pin of accelerometer
6	INTM	Interrupt pin of magnetometer
7	VDD	Power supply
8	GND_IO	Ground supply for I/O pins
9	GND	Ground supply
10	NC	
11	PS	This PIN must connect HIGH
12	SCL	I2C serial clock (SCL)

2 Module specifications

Mechanical characteristics

Table 2 Mechanical characteristic of accelerometer

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
A_FS	Measurement range	FS bit set to 00		±2		g
		FS bit set to 01		±4		g
		FS bit set to 10		±8		g
		FS bit set to 11		±16		g
A_So	Sensitivity	FS bit set to 00		4096		LSB/g
		FS bit set to 01		2048		LSB/g
		FS bit set to 10		1024		LSB/g
		FS bit set to 11		512		LSB/g
A_TCSo	Sensitivity change vs. temperature	FS bit set to 00		0.01		%/°C
A_TyOff	Typical zero-g level offset accuracy after SMT			150		mg
A_TCOff	Zero-g level change vs. temperature	Max delta from 25°C		±1		mg/°C
An	Acceleration noise density	FS bit set to 00, Normal Mode		150	200	ug/sqrt(Hz)
Top	Operation temperature range		-40		85	°C

Accelerometer specification parameter are specified VDD = 2.5 V, VDDIO = 2.5V T = 25 °C

Unless otherwise noted (a)

a. The product is factory calibrated at 2.5 V. The operational power supply range is from 2.2V to 3.6 V.

Table 3 Mechanical characteristic of magnetometer

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
M_FS	Measurement range			±48		Gauss
M_So	X/Y axis Sensitivity			667		LSBs/Gauss
	Z axis Sensitivity			400		LSBs/Gauss
M_NL	Non Linearity			0.1		% of FS
T_{CONV}	Conversion time		1		128	ms
T_{STBY}	From IDLE to STBY			250		us
T_{ACTIVE}	From STBY to ACTIVE			8		us
$T_{INTERVAL}$	Time between 2 conversions (burst mode or wake-up on change)		20		5000	ms

Magnetometer specification parameter are specified VDD=3.0V,VDD_IO=3.0V and T=25 ℃

Electrical characteristics

Table 4.Electrical characteristics of accelerometer

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
VDD	Supply voltage		1.62	2.5	3.6	V
VDD_IO	I/O Pins supply voltage		1.62		3.6	V
Idd	current consumption in normal mode	Top=25℃, ODR=1kHz		180		uA
Idd_lp	current consumption in low power mode	Top=25℃, ODR=62.5Hz, BW=500Hz		32		uA
Idd_sm	current consumption in suspend mode	Top=25℃		1		uA
VIH	Digital high level input voltage	I2C	0.7*VDD_IO			V
VIL	Digital low level input voltage	I2C			0.3*VDD_IO	V
VOH	high level output voltage		0.9*VDD_IO			V
VOL	Low level output voltage				0.1*VDD_IO	V
BW	System bandwidth		1.95		500	Hz
ODR	Output data rate		1		1000	Hz
Wake-up time	twu	From stand-by		1		ms
Start-up time	tsu	From power off		3		ms
PSRR	Power Supply Rejection Rate	Top=25℃			20	mg/V

The specifications are applicable at 25 ℃, unless specified otherwise, and for the complete supply voltage range(VDD=2.2V to 3.6V,VDD_IO=1.65V to VDD).

Table 5 Electrical characteristics of magnetometer

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
VDD	Analog Supply Voltage		2.2	3	3.6	V
VIO	Digital IO Supply		1.71	1.8	VDD	V
$IDD_{,CONV}$	Conversion Current			2.35	2.6	mA
$IDD_{,STBY}$	Standby Current			40		μA
$IDD_{,IDLE}$	Idle Current			2	3	μA
$IDD_{,NOM}$	Nominal Current (Data-rate = 10Hz, TCONV = 4ms)			280	320	μA

The specifications are applicable at 25 ℃,unless specified otherwise, and for the complete supply voltage range(VDD=2.2V to 3.6V,VDD_IO=1.65V to VDD).

Absolute maximum ratings

Table 6.Absolute maximum ratings for accelerometer

Parameter	Test conditions	Min	Max	Unit
Storage Temperature		-45	125	℃
Supply Voltage	Supply pins	-0.3	4.25	V
Supply Voltage	Logic pins	-0.3	VDD_IO+0.3	V
ESD Rating	HMB,R=1.5k,C=100pF		±2	kV
Mechanical Shock	Duration<200us		10,000	g

Table 7 Absolute maximum ratings for magnetometer

Parameter	Symbol	Min.	Max.	Unit
Power supply voltage	VDD	2.2V	3.6V	V
I/O pins supply voltage	VDD_IO	1.71V	VDD	V
Operating temperature range	TOP	-40	85	℃
Storage temperature range	TST	-50	125	℃
Electrostatic discharge protection: Human Body Model	ESD_HBM		2	KV
Electrostatic discharge protection: Machine Model	ESD_MM		N/A	V
Electrostatic discharge protection: Charged Device Model	ESD_CMD		750	V

Note: *Supply voltage on any pin should never exceed 4.25V*

Stresses above those listed as "Absolute maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.


This is a mechanical shock sensitive device, improper handling can cause permanent damages to the part.


This is an ESD sensitive device, improper handling can cause permanent damages to the part.

3 Communication interface

Communication interface Electrical specification

1.1.1 I2C Electrical specification

Table 8.Electrical specification of the I2C interface pins

Symbol	Parameter	Min	Max	Unit
fscl	Clock frequency		400	kHz
tscl_l	SCL low pulse	1.3		us
tscl_h	SCL high pulse	0.6		us
Tsda_setup	SDA setup time	0.1		us
Tsda_hold	SDA hold time	0.0		us
tsusta	Setup Time for a repeated start condition	0.6		us
thdsta	Hold time for a start condition	0.6		us
tsusto	Setup Time for a stop condition	0.6		us
tbuf	Time before a new transmission can start	1.3		us

The figure below shows the definition of the I2C timing given in Table 6:

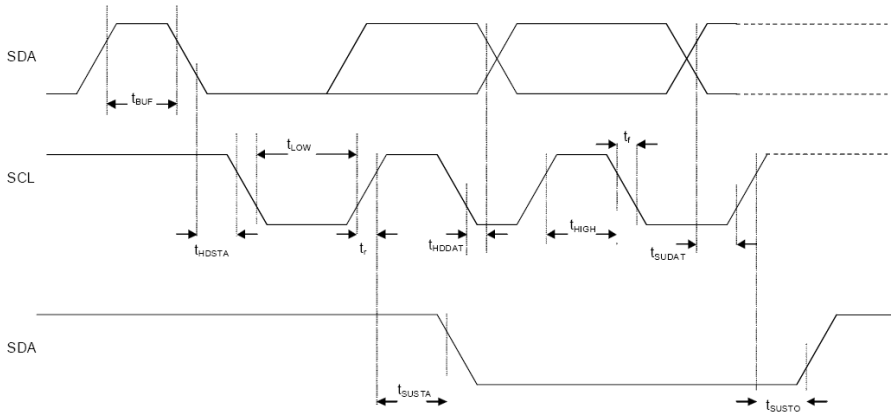


Figure 2 I2C Slave timing diagram

Digital interface operation

For accelerometer and magnetometer modules, the dc213 supports I2C serial digital interface protocols

1.1.2 I2C Operation

I2C bus uses SCL and SDA as signal lines. Both lines are connected to VDDIO externally via pull-up resistors so that they are pulled high when the bus is free. The dc213 include two I2C device address (for accelerometer and magnetometer) which is shown below.

1.1.2.1 I2C operation for accelerometer

The LSB bit of the 7bits device address is configured via SA0 pin.

Table 9.I2C Address for accelerometer

SAD6	SAD5	SAD4	SAD3	SAD2	SAD1	SAD0	W/ R
0	1	0	0	1	1	SAO	0/1

Table 10.SAD+Read/Write patterns

Command	SAD[6:1]	SAD[0]=SA0	R/W	SAD+R/W
Read	010011	0	1	01001101(4dh)
Write	010011	0	0	01001100(4ch)
Read	010011	1	1	01001111(4fh)
Write	010011	1	0	01001110(4eh)

The I2C interface protocol has special bus signal conditions. Start (S), stop (P) and binary data conditions are shown below. At start condition, SCL is high and SDA has a falling edge. Then the slave address is sent. After the 7 address bits, the direction control bit R/W selects the read or write operation. When a slave device recognizes that it is being addressed, it should acknowledge by pulling SDA low in the ninth SCL (ACK) cycle.

At stop condition, SCL is also high, but SDA has a rising edge. Data must be held stable at SDA when SCL is high. Data can change value at SDA only when SCL is low.

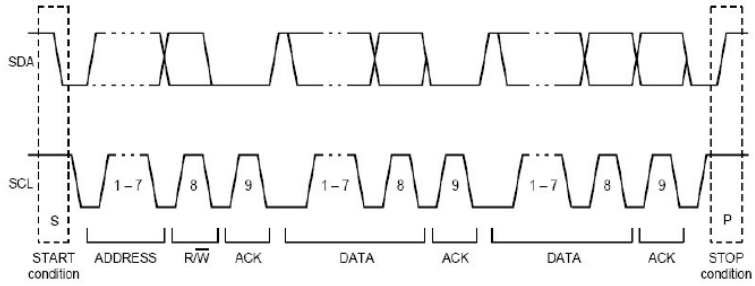


Figure 3 I2C Protocol

Table 11.Transfer when master is writing one byte to slave

Master	S	SAD+W		SUB		DATA		P
Slave			SAK		SAK		SAK	

Table 12.Transfer when master is writing multiple bytes to slave

Master	S	SAD+W		SUB		DATA		DATA		P
Slave			SAK		SAK		SAK		SAK	

Table 13.Transfer when master is receiving (reading) one byte of data from slave

Master	S	SAD+W		SUB		SR	SAD+R			NMASK	P
Slave			SAK		SAK			SAK	DATA		

Table 14.Transfer when master is receiving (reading) multiple bytes of data from slave

Master	S	SAD+W		SUB		SR	SAD+R			MAK		MAK		NMASK	P
Slave			SAK		SAK			SAK	DATA		DATA		DATA		

1.1.2.2 I2C operation for magnetometer

The I2C address of magnetometer is fixed as below

MSB							LSB
0	0	0	1	1	0	0	R/W

Command	EE_I2C_ADDR[4:0]	A1	A0	R/W	I2C _ADDR[6:0]+R/W
Read	00011	0	0	1	00011001(19H)
Write	00011	0	0	0	00011000(18H)

The device supports I2C communication in both standard mode and fast mode. Bytes are transmitted MSB first, and in order to reconstruct words, the bytes need to be concatenated MSByte first. The general principle of communication is always the same:

- Initiating the communication is always done by the Master (Start condition S).
- Addressing the Slave (dc213) followed by a cleared bit to indicate the Master intends to write something to the specific addressed Slave.
- Acknowledging by the Slave if the transmitted address corresponds to the Slave's I2C address. If the latter isn't the case, any further activity on the bus except a Sr (Start Repeat) and P (Stop) condition will be ignored by the dc213.
- Sending a Command Byte by the Master, as depicted in I2C Figure. The Slave will always acknowledge this, even if it is an unrecognized command.
- Issuing a Start Repeat (Sr) condition by the Master in order to restart the addressing phase
- Addressing the Slave (dc213) followed by a set bit to indicate the Master intends to read something from the specific addressed Slave
- Acknowledging by the Slave if the transmitted address corresponds to the Slave's I2C address. If the latter isn't the case, any further activity on the bus except a Sr (Start Repeat) and P (Stop) condition will be ignored by the dc213
- Transmitting the Status Byte by the Slave, who is in control of the bus
- Acknowledging by the Master if the data is well received
- Generating a Stop condition (P) by the master

The Master controlled bus activity is shown in grey body, the Slave controlled bus activity is shown in black body. In case a command is longer than a single byte (see command list), the bytes are transmitted sequentially before generating the Start Repeat (Sr) condition.

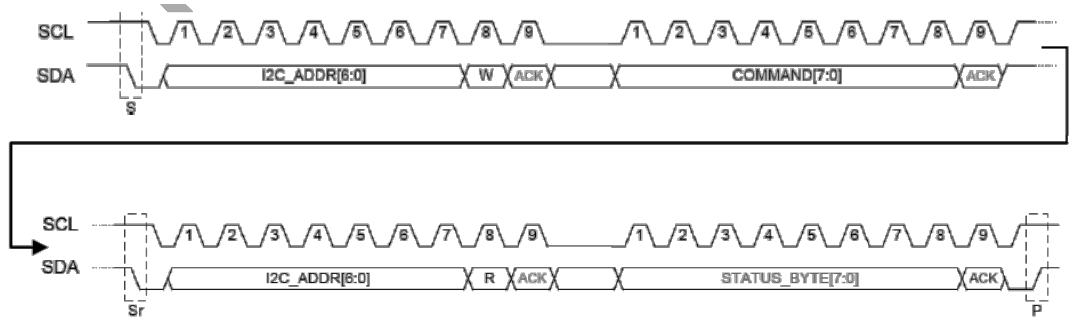


Figure 4 i2c protocol

The same applies to the Slave responses: following RR and RM commands, the Slave response is more than just the Status Byte. There as well, the data is partitioned in bytes that are transmitted sequentially by the slave. It is the Master's responsibility to issue enough clocking pulses to read back all the data. Finding out how many bytes is possible by decoding the Status Byte information, see Section Status Byte.

3.1.1.1.1 I2C slave timing values

Table 15 I2C slave timing values

Symbol	Parameter	Min	Max	Unit
fscl	Clock frequency		400	kHz
tscl_l	SCL low pulse	1.3		us
tscl_h	SCL high pulse	0.6		us
Tsda_setup	SDA setup time	0.1		us
Tsda_hold	SDA hold time	0.0		us
tsusta	Setup Time for a repeated start condition	0.6		us
thdsta	Hold time for a start condition	0.6		us
tsusto	Setup Time for a stop condition	0.6		us
tbuf	Time before a new transmission can start	1.3		us

Note:

1、 Data based on standard I2C protocol requirement, not tested in production.

2、 Cb=total capacitance of one bus line, in pF.

3.1.1.1.2 I2C slave timing diagram [note]

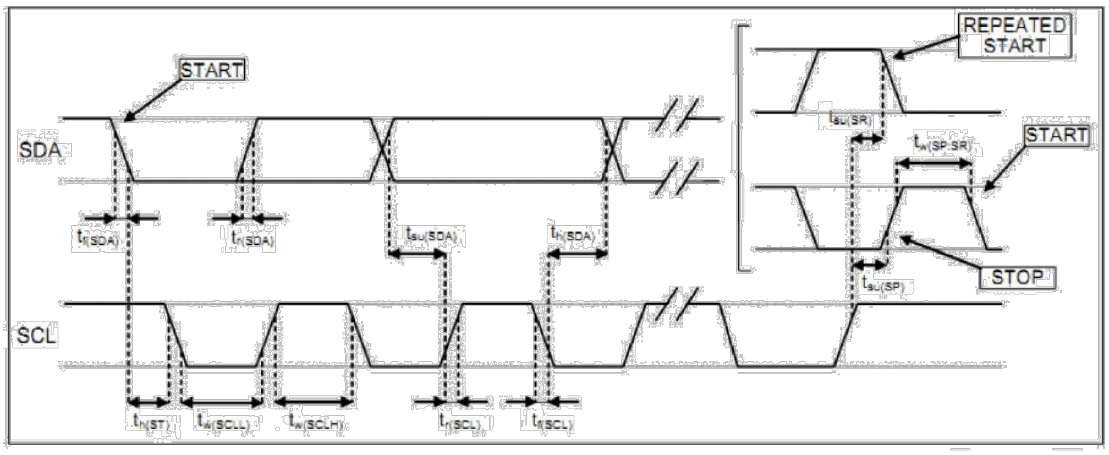


Figure 5 i2c slave timing

Note:

Measurement points are done at 0.2*VDD_IO and 0.8*VDD_IO, for both input and output port.

4 Terminology and functionality

Terminology

1.1.3 Sensitivity

Sensitivity describes the gain of the sensor and can be determined e.g. by applying 1 *g* acceleration to it. As the sensor can measure DC accelerations this can be done easily by pointing the axis of interest towards the center of the earth, noting the output value, rotating the sensor by 180 degrees (pointing to the sky) and noting the output value again. By doing so, ±1 *g* acceleration is applied to the sensor. Subtract the larger output value from the smaller one, and dividing the result by 2, leads to the actual sensitivity of the sensor. This value changes very little over temperature and also time. The sensitivity tolerance describes the range of sensitivities of a large population of sensors.

1.1.4 Zero-*g* level

Zero-*g* level offset (TyOff) describes the deviation of an actual output signal from the ideal output signal if no acceleration is present. A sensor in a steady state on a horizontal surface measure 0 *g* in X axis and 0 *g* in Y axis whereas the Z axis measure 1 *g*. The output is ideally in the middle of the dynamic range of the sensor (content of output data registers are 00h, data expressed as 2's complement number). A deviation from ideal value in this case is called Zero-*g* offset. Offset is to some extent a result of stress to MEMS sensor and therefore the offset can slightly change after mounting the sensor onto a printed circuit board or exposing it to extensive mechanical stress. Offset changes little over temperature; see "Zero-*g* level change vs. temperature". The Zero-*g* level tolerance (TyOff) describes the standard deviation of the range of Zero-*g* levels of a population of sensors.

Functionality of accelerometer

1.1.5 Power mode

The dc213 (accelerometer) has three different power modes. Besides normal mode, which represents the fully operational state of the device, there are two special energy saving modes: low-power mode and suspend mode.

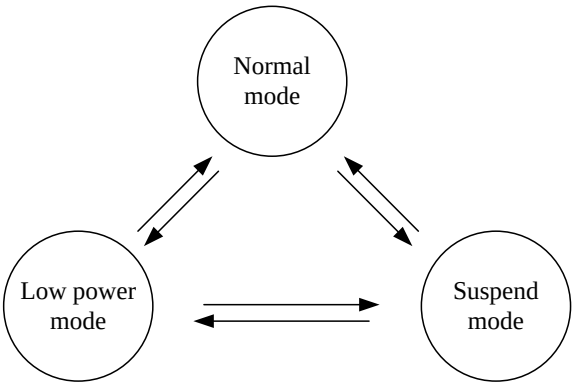


Figure 6 power mode

In normal mode, all parts of the electronic circuit are held powered-up and data acquisition is performed continuously.
In suspend mode, the whole analog part, including the oscillator, Ana LDO, Dig LDO and Drive Buffer are all powered down, no data acquisition is performed and the only supported operation is to read/write the registers. Suspend mode is entered by writing '11' or '10' to the (0x11) 'pwr_mode' bits.

In low power mode, the device is periodically switching between a sleep phase and a wake-up phase. The wake-up phase essentially corresponding to operation in normal mode with complete power-up of the circuitry. During the sleep phase the analog part except the oscillator is powered down.

During the wake-up phase, if a enabled interrupt is detected, the device stays in the wake-up phase as long as the interrupt condition endures (non-latched interrupt), or until the latch time expires (temporary interrupt), or until the interrupt is reset (latched interrupt). If no interrupt detected, the device enters the sleep phase.

1.1.6 Accelerometer data

The width of acceleration data is 14bits given in two's complement representation. The 14bits for each axis are split into an MSB part (one byte containing bits 13 to 6) and an LSB lower part (one byte containing bits 5 to 0)

1.1.7 Factory calibration

The IC is factory calibrated for sensitivity (So) and Zero-*g* level (TyOff). The trimming values are stored inside the chip's nonvolatile memory. The trimming parameters are loaded to registers while dc213 reset (POR or software reset). This allows using the device without further calibration.

1.1.8 Interrupt controller

Interrupt engines are integrated in the dc213. If the condition of an enabled interrupt is fulfilled, the corresponding status bit is set to 1 and the selected interrupt pin (INTA) is activated. The pin state is a logic 'or' combination of all

mapped interrupts.

1.1.8.1 General features

An interrupt is cleared depending on the selected interrupt mode, which is common to all interrupts. There are three different interrupt modes: non-latched, latched and temporary. The mode is selected by the 'latch_int' bits according to table19.

Table 16.Interrupt mode selection

latch_int	Interrupt mode
0000	non-latched
0001	temporary latched 250ms
0010	temporary latched 500ms
0011	temporary latched 1s
0100	temporary latched 2s
0101	temporary latched 4s
0110	temporary latched 8s
0111	latched
1000	non-latched
1001	temporary latched 1ms
1010	temporary latched 1ms
1011	temporary latched 2ms
1100	temporary latched 25ms
1101	temporary latched 50ms
1110	temporary latched 100ms
1111	latched

An interrupt is generated if its activation condition is met. It can't be cleared as long as the activation condition is fulfilled. In the non-latched mode the interrupt status bit and the selected pin (INTA) is cleared as soon as the activation condition is no more valid. Exceptions to this behavior are the new data and orientation, which are automatically reset after a fixed time.

In the latched mode an asserted interrupt status and the selected pin are cleared by writing 1 to (0x21) 'reset_int' bit. If the activation condition still holds when it is cleared, the interrupt status is asserted again with the next change of the acceleration registers.

In the temporary mode an asserted interrupt and selected pin are cleared after a defined period of time. The behavior of the different interrupt modes is shown in figure 9.

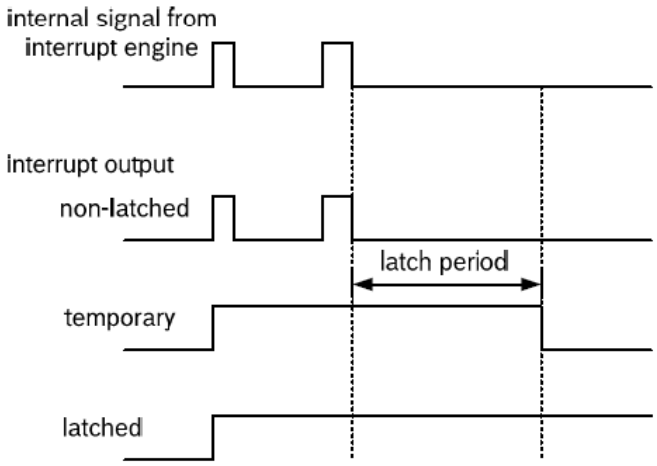


Figure 7 Interrupt mode

1.1.8.2 Mapping

The mapping of interrupts to the interrupt pins is done by registers 'INT_MAP_x' (0x19 0x1a and 0x1b), setting *inta_inttype* (e.g. inta_freefall) to 1 can map this type of interrupt to INTA pin.

1.1.8.3 Electrical behavior (INTA to open-drive or push-pull)

Both interrupt pins can be configured to show desired electrical behavior. The active level for each pin is set by register bit inta_lvl, if inta_lvl = 0 (1), then the pin INTA is 0 (1) active.
Also the electric type of the interrupt pin can be selected. By setting inta_od = 1 (0), the interrupt pin output type can be set to be open-drive (push-pull).

1.1.8.4 New data interrupt

This interrupt serves for synchronous reading of acceleration data. It is generated after an acceleration data was calculated. The interrupt is cleared automatically before the next acceleration data is ready.

1.1.8.5 Active detection

Active detection uses the slope between successive acceleration signals to detect changes in motion. An interrupt is generated when the slope (absolute value of acceleration difference) exceeds a preset threshold. The threshold is set with the value of register 'active_th' with the LSB corresponding to 16 LSB of acceleration data, that is 3.9mg in 2g-range, 7.8mg in 4g-range, 15.6mg in 8g-range and 31.3mg in 16g-range. And the maximum value is 1g in 2g-range, 2g in 4g-range, 4g in 8g-range and 8g in 16g-range.

The time difference between the successive acceleration signals depends is fixed to 1ms.

Active detection can be enabled (disabled) for each axis separately by writing '1' to bits 'active_int_en_x/y/z'. The active interrupt is generated if the slope of any of the enabled axes exceeds the threshold for ['active_dur'+1] consecutive times. As soon as the slopes of all enabled axes fall below this threshold for ['active_dur'+1] consecutive times, the interrupt is cleared unless the interrupt signal is latched.

The interrupt status is stored in the (0x09) 'active_int' bit. The (0x0b) bit 'active_first_x/y/z' records which axis triggered the active interrupt first and the sign of this acceleration data that triggered the interrupt is recorded in the (0x0b) bit 'active_sign'.

1.1.8.6 Tap detection

Tap detection has a functional similarity with a common laptop touch-pad or clicking keys of a computer mouse. A tap event is detected if a pre-defined pattern of the acceleration slope is fulfilled at least for one axis. Two different tap events are distinguished: A single tap is a single event within a certain time, followed by a certain quiet time. A double tap consist a first such event followed by a second event within a defined time.

Single tap interrupt is enabled by writing 1 to the (0x16) 's_tap_int_en' bit and double tap interrupt is enabled by writing 1 to the (0x16) 'd_tap_int_en' bit. The status of the single tap interrupt is stored in the (0x09) 's_tap_int' bit and the status of the double tap interrupt is stored in the (0x09) 'd_tap_int' bit.

The slope threshold for detecting a tap event is set by the (0x2b) "tap_th" bits with the LSB corresponding to 256LSB of acceleration data that is 62.5mg in 2g-range, 125mg in 4g-range, 250mg in 8g-range, 500mg in 16g-range. And the maximum value equals to the full scale in each range.

In figure10 the meaning of different timing parameter is visualized.

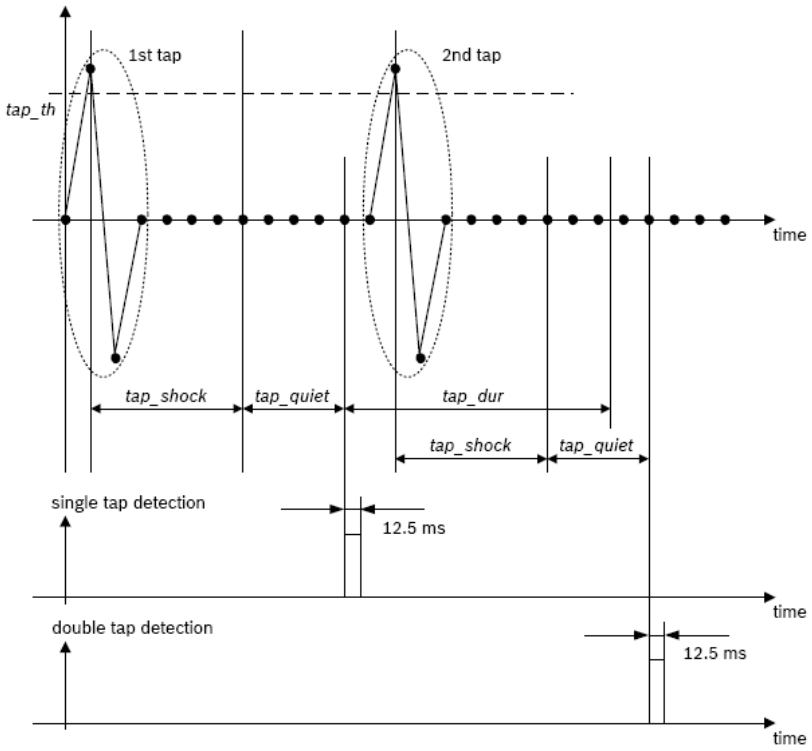


Figure 8 Timing of tap detection

The parameter 'tap_shock' and 'tap_quiet' apply to both single and double tap detection, while 'tap_dur' applies to double detection only. Within the duration of 'tap_shock' any slope exceeding 'tap_th' after the first event is ignored, within the duration of 'tap_quiet' there must be no slope exceeding 'tap_th', otherwise the first event will be cancelled.
A single tap is detected and the single tap interrupt is generated after the combination durations of 'tap_shock' and 'tap_quiet', if the corresponding slope conditions are fulfilled. The interrupt is cleared after a delay of 12.5ms in non-latched mode.

A double tap is detected and the double tap interrupt is generated if an event fulfilling the conditions for a single tap occurs within the set duration in 'tap_dur' after the completion of the first tap event. The interrupt is cleared after a delay in non-latched mode.

The sign of the slope of the first tap which triggered the interrupt is stored in the (0x0b) 'tap_sign' bit (0 means positive, 1 means negative). The axis which triggered the interrupt is indicated by the (0x0b) 'tap_first_x/y/z' bit.

Note: 'tap_shock' 'tap_quiet' 'tap_dur' 'tap_th' can be set by modifying register 0x2a and 0x2b

1.1.8.7 Orientation recognition

The orientation recognition feature informs on an orientation change of sensor with respect to the gravitation field vector 'g'. The measured acceleration vector components with respect to the gravitation field are defined as shown in

figure 11.

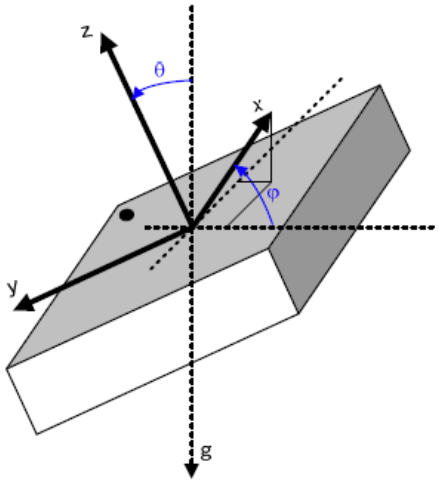


Figure 9 Definition of vector components

Therefore, the magnitudes of the acceleration vectors are calculated as follows:

$$acc\_x = 1g.\sin\theta\cdot\cos\varphi$$
$$acc\_y = -1g.\sin\theta\cdot\sin\varphi$$
$$acc\_z = 1g\cdot\cos\theta$$

Depending on the magnitudes of the acceleration vectors the orientation of the device in the space is determined and stored in the (0x09) 'orient_int' bit. There are three orientation calculation modes with different thresholds for switching between different orientations: symmetrical, high-asymmetrical and low-asymmetrical. The mode is selected by setting the (0x2c) 'orient_mode' bit. For each orientation mode, the 'orient' bits have a different meaning as show in table 17 to table 18.

Table 17.meaning of 'orient' bits in symmetric mode

orient	Name	Angle	Condition
X00	Portrait upright	$315^o < \varphi < 45^o$	|acc_y| < |acc_x| - 'hyst' &acc_x>= 0
X01	Portrait upside down	$135^o < \varphi < 225^o$	|acc_y| < |acc_x| - 'hyst' &acc_x< 0
X10	Landscape left	$45^o < \varphi < 135^o$	|acc_y| >= |acc_x| + 'hyst' & acc_y < 0
X11	Landscape right	$225^o < \varphi < 315^o$	|acc_y| >= |acc_x| + 'hyst' & acc_y >= 0

Table 18.meaning of 'orient' bits in high-asymmetric mode

Orient	Name	Angle	Condition
X00	Portrait upright	$297^o < \varphi < 63^o$	|acc_y| < 2*|acc_x| - 'hyst' &acc_x>= 0
X01	Portrait upside down	$117^o < \varphi < 243^o$	|acc_y| < 2*|acc_x| - 'hyst' &acc_x< 0
X10	Landscape left	$63^o < \varphi < 117^o$	|acc_y| >= 2*|acc_x| + 'hyst' & acc_y < 0
X11	Landscape right	$243^o < \varphi < 297^o$	|acc_y| >= 2*|acc_x| + 'hyst' & acc_y >= 0

Table 19.meaning of 'orient' bits in low-asymmetric mode

Orient	Name	Angle	Condition
X00	Portrait upright	$333^o < \varphi < 27^o$	|acc_y| < 0.5*|acc_x| - 'hyst' &acc_x>= 0

X01	Portrait upside down	$153^o < \varphi < 207^o$	|acc_y| < 0.5*|acc_x| - 'hyst' &acc_x< 0
X10	Landscape left	$27^o < \varphi < 153^o$	|acc_y| >= 0.5*|acc_x| + 'hyst' & acc_y < 0
X11	Landscape right	$207^o < \varphi < 333^o$	|acc_y| >= 0.5*|acc_x| + 'hyst' & acc_y >= 0

In the preceding tables, the parameter 'hyst' stands for a hysteresis which can be selected by the (0x2c) 'orient_hyst' bit. 1LSB of 'orient_hyst' always corresponds to 62.5mg in any g-range. The MSB of 'orient' bits contains information about the direction of the z-axis. It is set to 0(1) if acc_z>=0 (acc_z<0). The hysteresis for z axis is fixed to 0.2g.

The orient interrupt is enabled by writing the (0x16) 'orient_int_en' bit. The interrupt is generated if the value of 'orient' has changed. It is automatically cleared after one stable period of the orient value in non-latched mode. In temporary latched or latched mode, the orient value is kept fixed as long as the interrupt persists. After cleaning the interrupt, the 'orient' will updated with the next following value change.

The change of the 'orient' value and the generation of the interrupt can be blocked according to conditions selected by setting the value of the (0x2c) 'orient_block' bit as described by table20.

Table 20.blocking conditions for orientation recognition

orient_block	Conditions
00b	No blocking
01b	Z blocking
10b	Z blocking or acceleration slope in any axis > 0.2g
11b	No blocking

The Z blocking is defined by the following inequality:

$$|acc\_z| > z\_blocking$$

The parameter z_blocking of the above given equation stands for the contents of the (0x2d) 'z_blocking' bit. Hereby it is possible to define a blocking value between 0g and 0.9375g with an LSB = 0.0625g.

1.1.8.8 Freefall interrupt

This interrupt is based on the comparison of acceleration data against a low-g threshold. The interrupt is enabled by writing 1 to the (0x17) 'freefall_int_en' bit. There are two modes available: single mode and sum mode. In single mode the acceleration of each axis is compared with the threshold. In sum mode, the sum of absolute values of all accelerations |acc_x| + |acc_y| + |acc_z| is compared with the threshold. The mode is selected by the (0x24) 'freefall_mode' bit. The free fall threshold is set through the (0x23) 'freefall_th' bits with 1 LSB corresponding to an acceleration of 7.81mg. A hysteresis can be selected by setting the (0x24) 'freefall_hy' bits with 1 LSB corresponding to 125mg.

The freefall interrupt is generated if the absolute values of the acceleration of all axes or their sum are lower than the threshold for at least the time defined by the (0x22) 'freefall_dur' bits. The interrupt is reset if the absolute value of at least one axis or the sum is higher than the threshold plus the hysteresis for at least one data acquisition. The interrupt status is stored in the (0x09) 'freefall_int' bit.

Functionality of magnetometer

1.1.9 Operation Mode

The dc213 (magnetometer) can operate in 3 modes:

- Burst mode
- Single Measure mode
- Wake-Up on Change

1.1.9.1 Burst mode

The ASIC will have a programmable data rate (BURST_DATA_RATE [6:0] of ox01 register) at which it will operate. This data rate implies auto-wakeup and sequencing of the ASIC, flagging that data is ready on a dedicated pin (INTM). The maximum data rate will correspond to 1/n*TCONV (n=3) in case of 3 axes magnetic data. The time during which the ASIC has a counter running, but is not doing an actual conversion is called the Standby mode (STBY).

When the sensor is operating in burst mode, it will make conversions at specific time intervals. The programmability of the user is the following:

- Burst speed (TINTERVAL)
- Conversion time (TCONV)
- Axes/Temperature (MDATA)

Whenever the sensor has made the selected conversions (based on MDATA), the INTM pin will be set (active H) to indicate that the data is ready. It will remain high until the master has sent the command to read out at least one of the converted quantities (ZYXT). Should the master have failed to read out any of them by the time the sensor has made a new conversion, the INTM pin will be strobe low for 10us, and the next rising edge will indicate a new set of data is ready.

1.1.9.2 Single Measure mode

The master will ask for data via the corresponding protocol (I^2C), waking up the ASIC to make a single conversion, immediately followed by an automatic return to sleep mode (IDLE) until the next polling of the master. This polling can also be done by strobing the INTM pin, which has the same effect as sending a protocol command for a single measurement.

Whenever the sensor is set to this mode (or after startup) the sensor goes to the IDLE state where it awaits a

command from the master to perform a certain acquisition. The duration of the acquisition will be the concatenation of the T_{STBY}, T_{ACTIVE} and $n*T_{CONV}$ (n=numbers of axes). The conversion time will effectively be programmable by the user, but is equally a function of the required axes/temperature to be measured.

Upon reception of such a polling command from the master, the sensor will make the necessary acquisitions, and set the INTM pin high to signal that the measurement has been performed and the master can read out the data on the bus at his convenience. The INTM will be cleared either when:

- The master has issued a command to read out at least one of the measured components
- The master issues an Exit (EX) command to cancel the measurement
- The chip is reset, after POR (Power-on reset) or Reset command (RT)

1.1.9.3 Wake-Up on Change

This mode is similar to the burst mode in the sense that the device will be auto-sequencing, with the difference that the measured component(s) is/are compared with a reference and in case the difference is bigger than a user-defined threshold, the INTM pin is set. The user can select which axes and/or temperature fall under this cyclic check, and which thresholds are allowed.

The Wake-Up on Change (WOC) functionality can be set by the master with as main purpose to only receive an interrupt when a certain threshold is crossed. The WOC mode will always compare a new burst value with a reference value in order to assess if the difference between both exceeds a user-defined threshold. The reference value is defined as one of the following:

- The first measurement of WOC mode is stored as reference value once, as a result of a measurement. This measurement at “t=0”note1 is then the basis for comparison.
- The reference for acquisition (t) is always acquisition (t-1), in such a way that the INTM will only be set if the derivative of any component exceeds a threshold.

The in-application programmability is the same as for burst mode, but now the thresholds for setting the interrupt are also programmable by the user, as well as the reference, if the latter is data(t=0) or data(t-1)note1.

Note1:
WOC mode means when the device signal changes over threshold value, device interrupt pin will be pull-up high level and data output will be ready, or else device still keep in sleep mode.
There are two modes signal changes in data comparison:
1) The sampling data of current time (t) compare with the first sampling data of WOC mode.
2) The sampling data of current time (t) compare with the data of last time (t=t-1)

1.1.9.4 Change operating mode

The user can change the operating mode at all time through a specific command on the bus. The default start-up mode is Single Measurement mode (in IDLE state), but with a proper user command any mode can be set after power-up. Changing to Burst or WOC mode, coming from Single Measure mode is always accompanied by a measurement first. The top-level state diagram indicating the different modes and some relevant timing is shown below in this figure. In the Measure state, the MDATA flag will define which components will be measured (ZYXT). The sequential order can't be modified by the user.

Arrows indicated in grey are the direct result of a command to return to Single Measure mode. The main difference between STANDBY and WOC_IDLE is that in STANDBY mode, all analog circuitry is ready to make a conversion, but this is accompanied by a larger current consumption. For burst mode this extra current consumption is justified because the emphasis is more on accurate timing intervals, avoiding the delay of T_{STBY} before conversion.

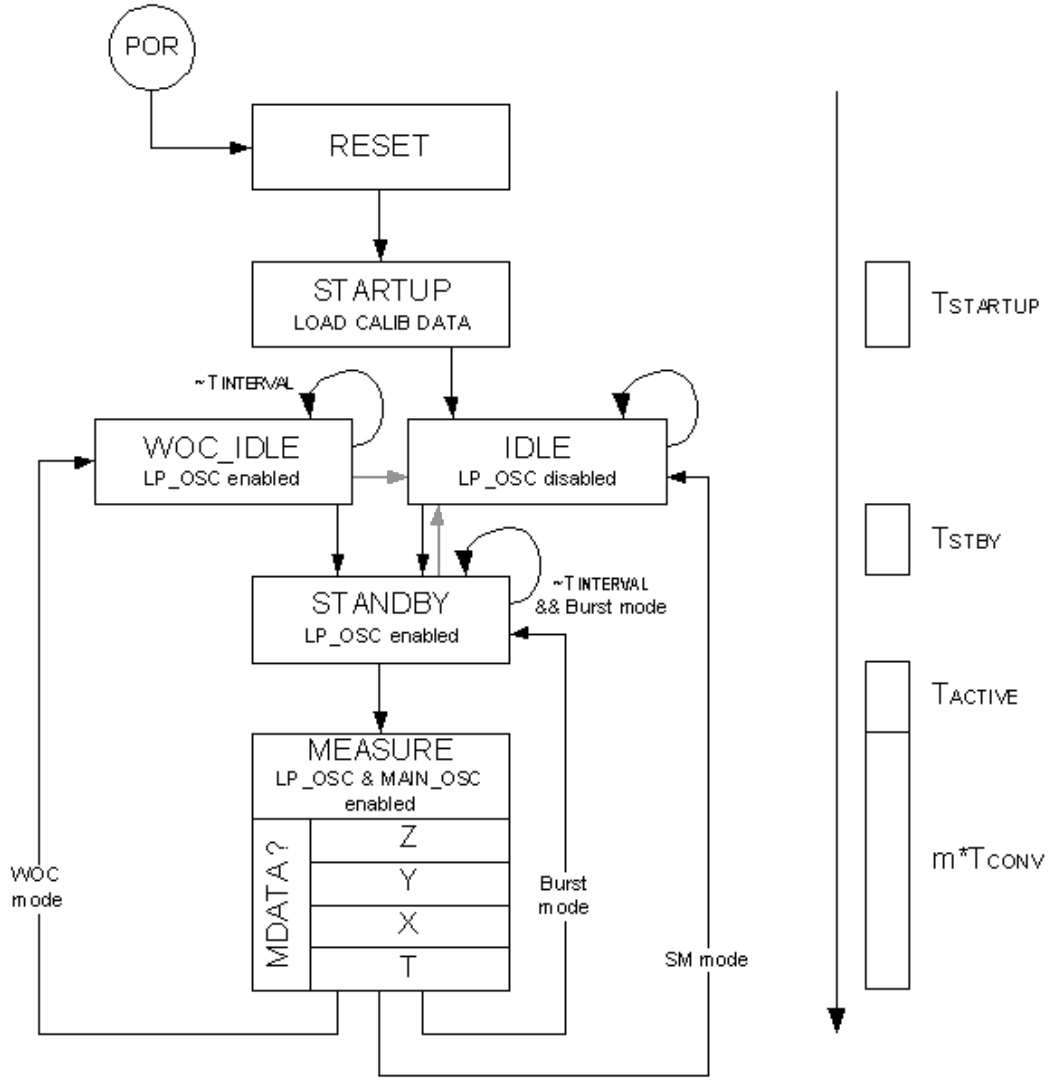


Figure 10 Operation mode

5 Application hints

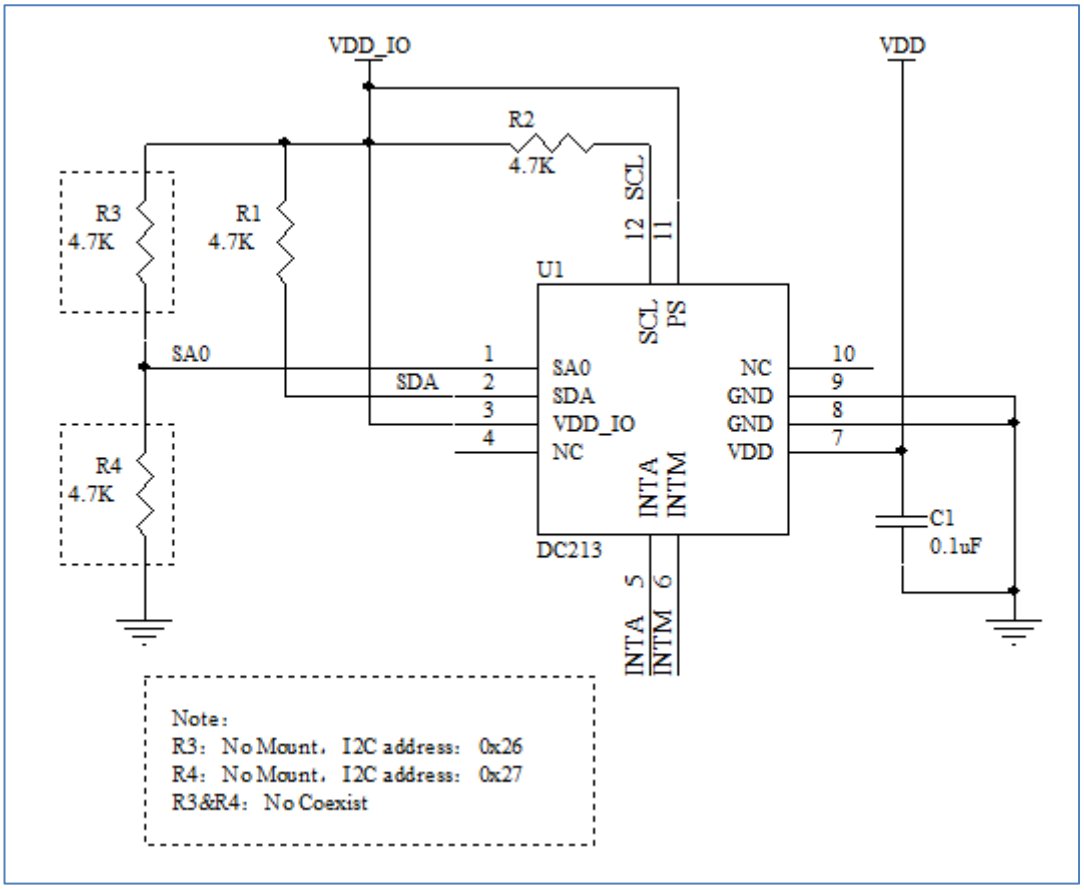


Figure 11 dc213 I2C electrical connection

The device core is supplied through VDD line while the I/O pads are supplied through VDD_IO line. Power supply decoupling capacitors (100 nF ceramic) should be placed as near as possible to the pin 7 and pin 3 of the device (common design practice).

The functionality of the device and the measured acceleration/magnetic data is selectable and accessible through the I2C interfaces. When using the I2C, PS must be tied high. The functions, the threshold and the timing of the two interrupt pins (INTA and INTM) can be completely programmed by the user through the I2C interface.

6 Register mapping for accelerometer

The table given below provides a listing of the 8 bit registers embedded in the device and the related addresses:

Table 21.Register address map

Name	Type	Register address	Default	Soft Reset
SOFT_RESET	RW	0x00	00H	NO
CHIPID	R	0x01	13H	NO
ACC_X_LSB	R	0x02	00H	NO
ACC_X_MSB	R	0x03	00H	NO
ACC_Y_LSB	R	0x04	00H	NO
ACC_Y_MSB	R	0x05	00H	NO
ACC_Z_LSB	R	0x06	00H	NO
ACC_Z_MSB	R	0x07	00H	NO
MOTION_FLAG	R	0x09	00H	NO
NEWDATA_FLAG	R	0x0A	00H	NO
TAP_ACTIVE_STATUS	R	0x0B	00H	NO
ORIENT_STATUS	R	0x0C	00H	NO
RESOLUTION_RANGE	RW	0x0F	00H	NO
ODR_AXIS	RW	0x10	0FH	YES
MODE_BW	RW	0x11	9EH	YES
SWAP_POLARITY	RW	0x12	00H	YES
INT_SET1	RW	0x16	10H	YES
INT_SET2	RW	0x17	00H	YES
INT_MAP1	RW	0x19	00H	YES
INT_MAP2	RW	0x1A	00H	YES
INT_CONFIG	RW	0x20	00H	YES
INT_LTACH	RW	0x21	00H	YES
FREEFALL_DUR	RW	0x22	09H	YES
FREEFALL_THS	RW	0x23	30H	YES
FREEFALL_HYST	RW	0x24	01H	YES
ACTIVE_DUR	RW	0x27	00H	YES
ACTIVE_THS	RW	0x28	14H	YES
TAP_DUR	RW	0x2A	04H	YES
TAP_THS	RW	0x2B	0AH	YES
ORIENT_HYST	RW	0x2C	18H	YES
Z_BLOCK	RW	0x2D	08H	YES
SELF_TEST	RW	0x32	00H	YES
CUSTOM_OFF_X	RW	0x38	00H	YES

CUSTOM_OFF_Y	RW	0x39	00H	YES
CUSTOM_OFF_Z	RW	0x3A	00H	YES
CUSTOM_FLAG	R	0x4E	00H	NO
CUSTOM_CODE	RW	0x4F	00H	YES
Z_CAL_EN	RW	0x50	00H	YES
Z_ROT_HODE_TM	RW	0x51	09H	YES
Z_ROT_DUR	RW	0x52	FFH	YES
ROT_TH_H	RW	0x53	45H	YES
ROT_TH_L	RW	0x54	35H	YES

7 Registers description for accelerometer

SOFT_RESET (00H)

Table 22. SOFT_RESET register

Default data: 0x00 Type: RW

SDO_Active	LSB_First	Soft_Reset	Unused	Unused	Soft Reset	LSB_First	SDO_Active

Table 23. I2C Configuration description

Soft_Reset	0: soft reset disable 1: soft reset enable

CHIPID (01h)

Table 24. CHIPID register

Default data: 0x13 Type: R

0	0	0	1	0	0	1	1

ACC_X_LSB (02H), ACC_X_MSB (03H)

X-axis acceleration data, the value is expressed in two complement byte and are left justified.

Table 25.ACC_X_LSB register

Default data: 0x00 Type: R

D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Unused	Unused

Table 26.ACC_X_MSB register

Default data: 0x00 Type: R

D[13]	D[12]	D[11]	D[10]	D[9]	D[8]	D[7]	D[6]

ACC_Y_LSB (04H), ACC_Y_MSB (05H)

Y-axis acceleration data, the value is expressed in two complement byte and are left justified.

Table 27.ACC_Y_LSB register

Default data: 0x00 Type: R

D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Unused	Unused

Table 28.ACC_Y_MSB register

Default data: 0x00 Type: R

D[13]	D[12]	D[11]	D[10]	D[9]	D[8]	D[7]	D[6]

ACC_Z_LSB (06H), ACC_Z_MSB (07H)

Z-axis acceleration data, the value is expressed in two complement byte and are left justified.

Table 29.ACC_Z_LSB register

Default data: 0x00 Type: R

D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Unused	Unused

Table 30.ACC_Z_MSB register

Default data: 0x00 Type: R

D[13]	D[12]	D[11]	D[10]	D[9]	D[8]	D[7]	D[6]

MOTION_FLAG (09H)

Table 31.MOTION_FLAG register

Default data: 0x00 Type: R

unused	orient_int	s_tap_int	d_tap_int	unused	active_int	unused	freefall_int

Table 32.MOTION_FLAG register description

orient_int	0:no orient interrupt 1:orient interrupt has occurred
s_tap_int	0:no single tap interrupt 1: single tap interrupt has occurred
d_tap_int	0:no double tap interrupt 1: double tap interrupt has occurred
active_int	0:no active interrupt 1: active interrupt has occurred
freefall_int	0:no freefall interrupt 1: freefall interrupt has occurred

NEWDATA_FLAG (0AH)

Table 33.NEWDATA_FLAG register

Default data: 0x00 Type: R

unused	unused	unused	unused	unused	unused	unused	new_data_int

Table 34.NEWDATA_FLAG register description

new_data_int	0: no new_data interrupt 1: new_data interrupt has occurred

TAP_ACTIVE_STATUS (0BH)

Table 35.TAP_ACTIVE_STATUS register

Default data: 0x00 Type: R

tap_sign	tap_first_x	tap_first_y	tap_first_z	active_sign	active_first_x	active_first_y	active_first_z

Table 36.TAP_ACTIVE_STATUS register description

tap_sign	Sign of the first tap that triggered interrupt 0: positive 1: negative
tap_first_x	0: X is not the triggering axis of the tap interrupt 1: indicate X is the triggering axis of the tap interrupt.
tap_first_y	0: Y is not the triggering axis of the tap interrupt 1: indicate Y is the triggering axis of the tap interrupt.
tap_first_z	0: Z is not the triggering axis of the tap interrupt 1: indicate Z is the triggering axis of the tap interrupt.
active_sign	active_sign: Sign of the 1st active interrupt. 0: positive, 1: negative
active_first_x	0: X is not the triggering axis of the active interrupt 1: indicate X is the triggering axis of the active interrupt.
active_first_y	0: Y is not the triggering axis of the active interrupt 1: indicate Y is the triggering axis of the active interrupt.
active_first_z	0: Z is not the triggering axis of the active interrupt 1: indicate Z is the triggering axis of the active interrupt.

ORIENT_STATUS (0CH)

Table 37.ORIENT_STATUS register

Default data: 0x00 Type: R

unused	orient[2]	orient[1]	orient[0]	unused	unused	unused	unused

Table 38.ORIENT_STATUS register description

Orient[2]	orientation value of 'z' axis 0: upward looking, 1: downward looking
Orient[1:0]	orientation value of 'x', 'y' axes 00: portrait upright 01: portrait upside down 10: landscape left 11:landscape right

RESOLUTION_RANGE (0FH)

Table 39.RESOLUTION_RANGE register

Default data: 0x00 Type: RW

unused	unused	unused	unused	resolution[1]	resolution[0]	fs[1]	fs[0]

Table 40.RESOLUTION_RANGE register description

resolution[1:0]	00:14bit 01:12bit 10:10bit 11:8bit
fs[1:0]	full scale 00: +/-2g 01: +/-4g 10:+/-8g 11:+/-16g

ODR_AXIS (10H)

Table 41.ODR_AXIS register

Default data: 0x0F Type: RW

X-axis_disable	Y-axis_disable	Z-axis_disable	unused	ODR[3]	ODR[2]	ODR[1]	ODR[0]

Table 42.ODR_AXIS register description

x-axis_disable	0: enable X axis 1: disable X axis
y-axis_disable	0: enable Y axis 1: disable Y axis
z-axis_disable	0: enable Z axis 1: disable Z axis
ODR[3:0]	0000: 1Hz (not available in normal mode) 0001: 1.95Hz (not available in normal mode) 0010: 3.9Hz 0011: 7.81Hz 0100: 15.63Hz 0101: 31.25Hz 0110: 62.5Hz 0111: 125Hz 1000: 250Hz 1001: 500Hz (not available in low power mode) 1010: 1000Hz (not available in low power mode) 1011-1111: 1000Hz

MODE_BW (11H)

Table 43.MODE_BW register

Default data: 0x9E Type: RW

pwr_mode [1]	pwr_mode [0]	unused	low_power_bw [3]	low_power_bw [2]	low_power_bw[1]	low_power_bw[0]	unused

Table 44.MODE_BW register description

pwr_mode[1:0]	00: normal mode, 01: low power mode, 1x: suspend mode.
low_power_bw [3:0]	0000-0010: 1.95Hz 0011: 3.9Hz 0100: 7.81Hz 0101: 15.63Hz 0110: 31.25Hz 0111: 62.5Hz 1000: 125Hz 1001: 250Hz 1010: 500Hz 1011-1111: 500Hz

SWAP_POLARITY (12H)

Table 45.SWAP_POLARITY register

Default data: 0x00 Type: RW

Swap & Polarity register is OTP register too, OTP address: 0x13

unused	unused	unused	unused	X_polarity	Y_polarity	Z_polarity	X_Y_swap

Table 46.SWAP_POLARITY register description

X_polarity	0: remain the polarity of X-axis. 1: reverse the polarity of X-axis.
Y_polarity	0: remain the polarity of Y-axis. 1: reverse the polarity of Y-axis.
Z_polarity	0: remain the polarity of Z-axis. 1: reverse the polarity of Z-axis.
X_Y_swap	0: Don’t need swap the output data for X/Y axis 1: swap the output data for X/Y axis.

INT_SET1 (16H)

Table 47.INT_SET1 register

Default data: 0x00 Type: RW

unused	orient_int_en	s_tap_int_en	d_tap_int_en	unused	active_int_en_z	active_int_en_y	active_int_en_x

Table 48.INT_SET1 register description

orient_int_en	0: disable the orient interrupt. 1: enable the orient interrupt.
s_tap_int_en	0: disable the single tap interrupt. 1: enable the single tap interrupt.
d_tap_int_en	0: disable the double tap interrupt. 1: enable the double tap interrupt.
active_int_en_z	0: disable the active interrupt for the z axis. 1: enable the active interrupt for the z axis.
active_int_en_y	0: disable the active interrupt for the y axis. 1: enable the active interrupt for the y axis.
active_int_en_x	0: disable the active interrupt for the x axis. 1: enable the active interrupt for the x axis.

INT_SET2 (17H)

Table 49.INT_SET2 register

Default data: 0x00 Type: RW

unused	unused	unused	new_data_int_en	freefall_int_en	unused	unused	unused

Table 50.INT_SET2 register description

new_data_int_en	0: disable the new data interrupt. 1: enable the new data interrupt.
freefall_int_en	0: disable the freefall interrupt. 1: enable the freefall interrupt

INT_MAP1 (19H)

Table 51.INT_MAP1 register

Default data: 0x00 Type: RW

unused	inta_orient	inta_s_tap	inta_d_tap	unused	inta_active	unused	inta_freefall

Table 52.INT_MAP1 register description

inta_orient	0: doesn’t mapping orient interrupt to INTA 1: mapping orient interrupt to INTA
inta_s_tap	0: doesn’t mapping single tap interrupt to INTA 1: mapping single tap interrupt to INTA
inta_d_tap	0: doesn’t mapping double tap interrupt to INTA 1: mapping double tap interrupt to INTA
inta_active	0: doesn’t mapping active interrupt to INTA 1: mapping active interrupt to INTA
inta_freefall	0: doesn’t mapping freefall interrupt to INTA 1: mapping freefall interrupt to INTA

INT_MAP2 (1AH)

Table 53.INT_MAP2 register

Default data: 0x00 Type: RW

unused	unused	unused	unused	unused	unused	unused	unused	inta_new_data

Table 54.INT_MAP2 register description

inta_new_data	0: doesn't mapping new data interrupt to INTA 1: mapping new data interrupt to INTA

INT_CONFIG (20H)

Table 55.INT_CONFIG register

Default data: 0x00 Type: RW

unused	unused	unused	unused	unused	unused	inta_od	inta_lvl

Table 56.INT_CONFIG register description

inta_od	0: select push-pull output for INTA 1: selects OD output for INTA
inta_lvl	0: selects active level low for pin INTA 1: selects active level high for pin INTA

INT_LTACH (21H)

Table 57.INT_LTACH register

Default data: 0x00 Type: RW

reset_int	unused	unused	unused	latch_int[3]	latch_int[2]	latch_int[1]	latch_int[0]

Table 58.INT_LTACH register description

reset_int	0: doesn't reset all latched int. 1: reset all latched int.
latch_int[3:0]	0000: non-latched 0001: temporary latched 250ms 0010: temporary latched 500ms 0011: temporary latched 1s 0100: temporary latched 2s 0101: temporary latched 4s 0110: temporary latched 8s 0111: latched 1000: non-latched 1001: temporary latched 1ms 1010: temporary latched 1ms 1011: temporary latched 2ms 1100: temporary latched 25ms 1101: temporary latched 50ms 1110: temporary latched 100ms

	1111: latched

FREEFALL_DUR (22H)

Table 59.FREEFALL_DUR register

Default data: 0x09 Type: RW

freefall_dur[7]	freefall_dur[6]	freefall_dur[5]	freefall_dur[4]	freefall_dur [3]	freefall_dur [2]	freefall_dur [1]	freefall_dur [0]

Table 60.FREEFALL_DUR register description

freefall_dur[7:0]	Delay time for freefall delay_time = (freefall_dur + 1) * 2ms range from 2ms to 512ms default: 20ms

FREEFALL_THS (23H)

Table 61.FREEFALL_THS register

Default data: 0x30 Type: RW

freefall_th[7]	freefall_th [6]	freefall_th [5]	freefall_th[4]	freefall_th [3]	freefall_th [2]	freefall_th [1]	freefall_th [0]

Table 62.FREEFALL_THS register description

freefall_th[7:0]	freefall threshold = freefall_th * 7.81mg LSB = 7.81mg default is 375mg

FREEFALL_HYST (24H)

Table 63.FREEFALL_HYST register

Default data: 0x01 Type: RW

unused	unused	unused	unused	unused	freefall_mode	freefall_hy[1]	freefall_hy[0]

Table 64.FREEFALL_HYST register description

freefall_mode	0: single mode. 1: sum mode.
freefall_hy[1:0]	Set the hysteresis for freefall detection. Free fall hysteresis time = freefall_hy* 125ms

	LSB = 125mg

ACTIVE_DUR (27H)

Table 65.ACTIVE_DUR register

Default data: 0x00 Type: RW

unused	unused	unused	unused	unused	unused	active_dur[1]	active_dur[0]

Table 66.ACTIVE_DUR register description

active_dur[1:0]	Active duration time = (active_dur + 1) ms

ACTIVE_THS (28H)

Table 67.ACTIVE_THS register

Default data: 0x14 Type: RW

active_th[7]	active_th [6]	active_th [5]	active_th[4]	active_th [3]	active_th [2]	active_th [1]	active_th [0]

Table 68.ACTIVE_THS register description

active_th[7:0]	Threshold of active interrupt=active_th*mg/LSB LSB = 3.91mg (2g range) LSB = 7.81mg (4g range) LSB = 15.625mg (8g range) LSB = 31.25mg (16g range)

TAP_DUR (2AH)

Table 69.TAP_DUR register

Default data: 0x04 Type: RW

tap_quiet	tap_shock	unused	unused	unused	tap_dur[2]	tap_dur[1]	tap_dur[0]

Table 70.TAP_DUR register description

tap_quiet	0: tap quiet duration 30ms. 1: tap quiet duration 20ms.
tap_shock	0: tap shock duration 50ms. 1: tap shock duration 70ms.
tap_dur[2:0]	Tap duration selects the length of the time window for the second shock. 000: 50ms 001: 100ms 010: 150ms 011: 200ms 100: 250ms 101: 375ms 110: 500ms 111: 700ms

TAP_THS (2BH)

Table 71.TAP_THS register

Default data: 0x0a Type: RW

unused	unused	unused	tap_th [4]	tap_th [3]	tap_th [2]	tap_th [1]	tap_th [0]

Table 72.TAP_THS register description

tap_th [4:0]	Threshold of tap interrupt=Tap_th*mg/LSB LSB = 62.5mg (2g range) LSB = 125mg(4g range) LSB = 250mg(8g range) LSB = 500mg (16g range)

ORIENT_HYST (2CH)

Table 73.ORIENT_HYST register

Default data: 0x18 Type: RW

unused	orient_hyst[2]	orient_hyst[1]	orient_hyst[0]	orient_block[1]	orient_block [0]	orient_mode [1]	orient_mode [0]

Table 74.ORIENT_HYST register description

orient_hyst[2:0]	Set the hysteresis of the orientation interrupt 1LSB = 62.5mg.
orient_block[1:0]	00: no blocking 01: z blocking 10: z blocking or slope in any axis > 0.2g 11: no blocking
orient_mode [1:0]	00: symmetrical 01: high-asymmetrical 10: low-asymmetrical 11:synmmetrical

Z_BLOCK (2DH)

Table 75.Z_BLOCK register

Default data: 0x08 Type: RW

unused	unused	unused	unused	z_blocking[3]	z_blocking[2]	z_blocking[1]	z_blocking[0]

Table 76.Z_BLOCK register description

z_blocking[3:0]	Defines the blocking acc_z between 0g to 0.9375g degree. 1LSB=62.5mg

CUSTOM_OFF_X (38H)

Table 77.CUSTOM_OFF_X register

Default data: 0x00 Type: RW

CUSTOM_OFF_X register is OTP register too, OTP address: 0x1D

cust_off_X[7]	cust_off_X[6]	cust_off_X[5]	cust_off_X[4]	cust_off_X[3]	cust_off_X[2]	cust_off_X[1]	cust_off_X[0]

Table 78.CUSTOM_OFF_X register description

cust_off_X[7:0]	customer offset compensation value for X axis LSB=3.9mg

CUSTOM_OFF_Y (39H)

Table 79.CUSTOM_OFF_Y register

Default data: 0x00 Type: RW

CUSTOM_OFF_Y register is OTP register too, OTP address: 0x1E

cust_off_Y[7]	cust_off_Y[6]	cust_off_Y[5]	cust_off_Y[4]	cust_off_Y[3]	cust_off_Y[2]	cust_off_Y[1]	cust_off_Y[0]

Table 80.CUSTOM_OFF_Y register description

cust_off_Y[7:0]	customer offset compensation value for Y axis LSB=3.9mg

CUSTOM_OFF_Z (39H)

Table 81.CUSTOM_OFF_Z register

Default data: 0x00 Type: RW

CUSTOM_OFF_Z register is OTP register too, OTP address: 0x1F

cust_off_Z[7]	cust_off_Z[6]	cust_off_Z[5]	cust_off_Z[4]	cust_off_Z[3]	cust_off_Z[2]	cust_off_Z[1]	cust_off_Z[0]

Table 82.CUSTOM_OFF_Z register description

Custom_offset_Z[7:0]	customer offset compensation value for Z axis LSB=3.9mg

CUSTOM_FLAG (4EH)

Table 83.CUSTOM_FLAG register

Default data: 0x00 Type: R

unused	unused	unused	unused	unused	unused	unused	custom_OTP_programmed

Table 84.CUSTOM_FLAG register description

custom_OTP_programmed	0: Custom OTP is not be programmed 1: Indicate the custom OTP is already programmed and can't be programmed again

CUSTOM_CODE (4FH)

Table 85.CUSTOM_CODE register

Default data: 0x00 Type: RW

custom_OTP_program[5]	custom_OTP_program[4]	custom_OTP_program[3]	custom_OTP_program[2]	custom_OTP_program[1]	custom_OTP_program[0]	custom_Pre_program	unused

Table 86.CUSTOM_CODE register description

custom_OTP_program	Write 0x9a to the register start customer OTP program

Z_ROT_HODE_TM (51H)

Table 87.Z_ROT_HODE_TM register

Default data: 0x09 Type: RW

z_rot_hold_time[7]	z_rot_hold_time[6]	z_rot_hold_time[5]	z_rot_hold_time[4]	z_rot_hold_time[3]	z_rot_hold_time[2]	z_rot_hold_time[1]	z_rot_hold_time[0]

Table 88.Z_ROT_HODE_TM register description

z_rot_hold_time[7:0]	Set the hold time for Z-axis rotation detecting. LSB = 1ms

Z_ROT_DUR (52H)

Table 89.Z_ROT_DUR register

Default data: 0xff Type: RW

z_rot_dur[7]	z_rot_dur[6]	z_rot_dur[5]	z_rot_dur[4]	z_rot_dur[3]	z_rot_dur[2]	z_rot_dur[1]	z_rot_dur[0]

Table 90.Z_ROT_DUR register description

z_rot_hold_time[7:0]	Set the duration time between twice z-axis rotating detecting. LSB = 4ms

ROT_TH_H (53H)

Table 91.ROT_TH_H register

Default data: 0x45 Type: RW

Rot_th_h [7]	Rot_th_h [6]	Rot_th_h [5]	Rot_th_h [4]	Rot_th_h [3]	Rot_th_h [2]	Rot_th_h [1]	Rot_th_h [0]

Table 92.ROT_TH_H register description

Rot_th_h [7:0]	Set the higer threshold value for (X^2+Y^2) to indicate once Z-rotaion, LSB = 15.6mg

ROT_TH_L (54H)

Table 93.ROT_TH_L register

Default data: 0x35 Type: RW

Rot_th_l [7]	Rot_th_l[6]	Rot_th_l[5]	Rot_th_l[4]	Rot_th_l [3]	Rot_th_l [2]	Rot_th_l [1]	Rot_th_l [0]

Table 94.ROT_TH_L register description

Rot_th_l [7:0]	Set the lower threshold value for (X^2+Y^2) to indicate once Z-rotaion, LSB = 15.6mg

8 Register mapping for magnetometer

The latter can be filled with customer content freely, and covers the address span from (and including) 0x0Ah to 0x1Fh, a total of 352 bits. The memory mapping of volatile and non-volatile memory on address level is identical. The volatile memory map is given in this table.

Table 95 Register for magnetometer

	Bit Number															
Address	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x00	ANA_RESERVED_LOW							BIST		GAIN_SEL			HALLCONF			
0x01	TRIG/INT	COMM_MODE		WOC_DIFF	EXT_TRIG	TCMP_EN	BURST_SET(zyxt)			BURST_DATA_RATE						
0x02				OSR2		RES_XYZ						DIG_FILT			OSR	
0x03	SENS_TC_HT								SENS_TC_LT							
0x04	OFFSET_X															
0x05	OFFSET_Y															
0x06	OFFSET_Z															
0x07	WOXY_THRESHOLD															
0x08	WOZ_THRESHOLD															
0x09	WOT_THRESHOLD															

9 Register description for magnetometer

The meaning of each customer accessible parameter is explained in this section. The customer area of both the volatile and the non-volatile memory can be written through standard I^2C communication, within the application. No external high-voltages are needed to perform such operations, nor access to dedicated pins that need to be grounded in the application.

Register:0x00

MSByte:

BIT15	BIT14	BIT13	BIT12	BIT11	BIT10	BIT9	BIT8
ANA_RESERVED_LOW							BIST

LSByte:

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
0	GAIN_SEL[2]	GAIN_SEL[1]	GAIN_SEL[0]	HALLCONF[3]	HALLCONF[2]	HALLCONF[1]	HALLCONF[0]

Register(0x00) description

ANA_RESERVED_LOW	Reserved IO trimming bits
BIST	Enabled the on-chip coil, applying a Z-field [Built-In Self Test][note1] 0: normal 1: generate magnetic field for self-test
0	undefined bit
GAIN_SEL[2:0]	Analog chain gain setting, factor 5[note2] between min and max code
HALLCONF[3:0]	Hall plate spinning rate adjustment

GAIN_SEL specify the gain of the analog chain (relative to GAIN_SEL=0)

GAIN_SEL<2:0>	Multiplication
0	1
1	1.25
2	1.66
3	2
4	2.5
5	3
6	3.75
7	5

Note:

1:When the BIST=1, Self test mode is enabled, in this mode we can detect magnetic output of Z axis to acknowledge de vice status. Pls refer to application note to know how to detect device in self test mode.

2: factor 5 is multiplication between GAIN_SEL=7(MAX) and GAIN_SEL=0(MIN).

Register:0x01

MSByte:

BIT15	BIT14	BIT13	BIT12	BIT11	BIT10	BIT9	BIT8
TRIG/INT	COMM_MODE[1]	COMM_MODE[0]	WOC_DIFF	EXT_TRIG	TCMP_EN	BURST_SET(zyxt)[z]	BURST_SET(zyxt)[y]

LSByte:

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
BURST_SET (zyxt)[x]	BURST_SET (zyxt)[t]	BURST_DATA _RATE[5]	BURST_DATA _RATE[4]	BURST_DATA _RATE[3]	BURST_DATA _RATE[2]	BURST_DATA _RATE[1]	BURST_DATA _RATE[0]

Register (0x01) description

TRIG/INT	Puts TRIG_INT pin in TRIG mode when cleared, INT mode otherwise
COMM_MODE[1:0]	Allow only I^2C [11b]
WOC_DIFF	Sets the Wake-up On Change based on Δ{sample(t),sample(t-1)} 0: The sampling data of current time (t) compare with the first sampling data of WOC mode. 1: The sampling data of current time (t) compare with the data of last time (t=t-1)
EXT_TRIG	Allows external trigger inputs when EXT_TRIG is set, if TRIG/INT = 0
TCMP_EN	Enables on-chip sensitivity drift compensation
BURST_DATARATE[6:0]	Defines TINTERVAL as BURST_DATA_RATE * 20ms

Register:0x02

MSByte:

BIT15	BIT14	BIT13	BIT12	BIT11	BIT10	BIT9	BIT8
			OSR2[1]	OSR2[0]	RES_XYZ_Z[1]	RES_XYZ_Z[0]	RES_XYZ_Y[1]

LSByte:

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
RES_XYZ_Y[0]	RES_XYZ_X[1]	RES_XYZ_X[0]	DIG_FILT[2]	DIG_FILT[1]	DIG_FILT[0]	OSR[1]	OSR[0]

Register(0x02) description

OSR2[1:0]	Temperature sensor ADC oversampling ratio
RES_XYZ[5:0]	Selects the desired 16-bit output value from the 19-bit ADC Every direction(X/Y/Z) has its own 2-bit parameter
DIG_FILT[2:0]	Digital filter applicable to ADC
OSR[1:0]	Magnetic sensor ADC oversampling ratio

RES_XYZ specify the resolution of the measurement：

The output of ADC is unsigned 19bits data. The output of the sensor would be 16bits which is selected from 19bits. Please refer to the table below:

Unsigned 16 bits sensor output (B_{OUT}):

RES_x/y/z<1:0>																			
0	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
2	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
3	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Change unsigned 16bits to signed 16bits:

RES_i	Unsigned 16bits	Signed 16bits
0	B_{OUT}	B_{OUT}
1	B_{OUT}	B_{OUT}
2	B_{OUT}	$B_{OUT}-2^{15}$
3	B_{OUT}	$B_{OUT}-2^{14}$

Register:0x03

MSByte:

BIT15	BIT14	BIT13	BIT12	BIT11	BIT10	BIT9	BIT8
SENS_TC_HT[7]	SENS_TC_HT[6]	SENS_TC_HT[5]	SENS_TC_HT[4]	SENS_TC_HT[3]	SENS_TC_HT[2]	SENS_TC_HT[1]	SENS_TC_HT[0]

LSByte:

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
SENS_TC_LT[7]	SENS_TC_LT[6]	SENS_TC_LT[5]	SENS_TC_LT[4]	SENS_TC_LT[3]	SENS_TC_LT[2]	SENS_TC_LT[1]	SENS_TC_LT[0]

Register(0x03) description

SENS_TC_HT[7:0]	Sensitivity drift compensation factor for $T < T_{REF}$
SENS_TC_LT[7:0]	Sensitivity drift compensation factor for $T > T_{REF}$

Register:0x04

BIT15	BIT14	BIT13	BIT12	BIT11	BIT10	BIT9	BIT8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
OFFSET_X[15:0]															

Register (0x04) description

OFFSET_X[15:0]	Constant X-offset correction

Register:0x05

BIT15	BIT14	BIT13	BIT12	BIT11	BIT10	BIT9	BIT8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
OFFSET_Y[15:0]															

Register (0x05) description

OFFSET_Y[15:0]	Constant Y-offset correction

Register:0x06

BIT15	BIT14	BIT13	BIT12	BIT11	BIT10	BIT9	BIT8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
OFFSET_Z[15:0]															

Register (0x06) description

OFFSET_Z[15:0]	Constant Z-offset correction

Register:0x07

BIT15	BIT14	BIT13	BIT12	BIT11	BIT10	BIT9	BIT8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
WO_XY_THRESHOLD[15:0]															

Register (0x07) description

WO_XY_THRESHOLD[15:0]	Wake-up On Change XY-threshold

Register:0x08

BIT15	BIT14	BIT13	BIT12	BIT11	BIT10	BIT9	BIT8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
WO_Z_THRESHOLD[15:0]															

Register (0x08) description

WO_Z_THRESHOLD[15:0]	Wake-up On Change Z-threshold

Register:0x09

BIT15	BIT14	BIT13	BIT12	BIT11	BIT10	BIT9	BIT8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
WO_T_THRESHOLD[15:0]															

Register (0x09) description

WO_T_THRESHOLD[15:0]	Wake-up On Change T-threshold

Command List

The dc213 only listens to a specific set of commands. Apart from the Reset command, all commands generate a status byte that can be read out. The table below indicates the 12 different commands that are (conditionally) accepted by the dc213.

1.1.10Command Table

Command					
Command Name	**Symbol**	**CMD1 byte(3)**	**CMD2 byte(3)**	**CMD3 byte(3)**	**CMD4 byte(3)**
No Operation	NOP	0000 0000	N/A	N/A	N/A
Start Burst Mode	SB	0001 zyxt(1)	N/A	N/A	N/A
Start Wake-up on Change Mode	SW	0010 zyxt(1)	N/A	N/A	N/A
Start Single Measurement Mode	SM	0011 zyxt(1)	N/A	N/A	N/A
Read Measurement	RM	0100 zyxt(1)	N/A	N/A	N/A
Read Register	RR	0101 0abc(2)	{A5… A0 ,0,0}	N/A	N/A
Write Register	WR	0110 0abc(2)	D 15 …D8	D 7… D0	{A5… A0 ,0 ,0 }
Exit Mode	EX	1000 0000	N/A	N/A	N/A
Memory Recall	HR	1101 0000	N/A	N/A	N/A
Memory Store	HS	1110 0000	N/A	N/A	N/A
Reset	RT	1111 0000	N/A	N/A	N/A

Note:

1. The argument in all mode-starting commands (SB/SW/SM) is a nibble specifying the conversions to be performed by the sensor in the following order «zyxt». For example, if only Y axis and temperature are to be measured in Single Measurement mode the correct command to be transmitted is 0x35h.
2. The argument for the volatile memory access commands (RR/WR) «abc» should be set to 0x0h, in order to get normal read-out and write of the memory.
3. CMD byte have to been sent before start repeat.

1.1.11Status byte

The status byte is the first byte transmitted by the dc213 in response to a command issued by the master. It is composed of a fixed combination of informative bits:

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
BURST_MODE	WOC_MODE	SM_MODE	ERROR	SED	RS	D1	D0

MODE bits

These bits define in which mode the dc213 is currently set. Whenever a mode transition command is rejected, the first status byte after this command will have the expected mode bit cleared, which serves as an indication that the command has been rejected, next to the ERROR bit. The SM_MODE flag can be the result of an SM command or from raising the TRIG pin when TRIG mode is enabled in the volatile memory of the dc213.

ERROR bit

This bit is set in case a command has been rejected or in case an uncorrectable error is detected in the memory, a so called ECC_ERROR. A single error in the memory can be corrected (see SED bit), two errors can be detected and will generate the ECC_ERROR. In such a case all commands but the RT (Reset) command will be rejected.

SED bit

The single error detection bit simply flags that a bit error in the non-volatile memory has been corrected. It is purely informative and has no impact on the operation of the dc213.

RS bit

Whenever the dc213 gets out of a reset situation – both hard and soft reset – the RS flag is set to highlight this situation to the master in the first status byte that is read out. As soon as the first status byte is read, the flag is cleared until the next reset occurs.

D[1:0] bits

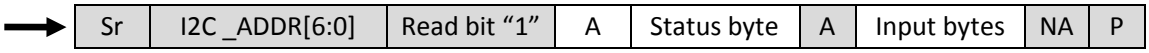
These bits only have a meaning after the RR and RM commands, when data is expected as a response from the dc213. The number of response bytes correspond to 2*D[1:0] + 2, so the expected byte counts are either 2, 4, 6 or 8.

1.1.12Command Usage:

All of the command usage should follow the sequence, each command has its own input and output bytes, output byte can be found in the command list table, only RR and RM has input bytes.

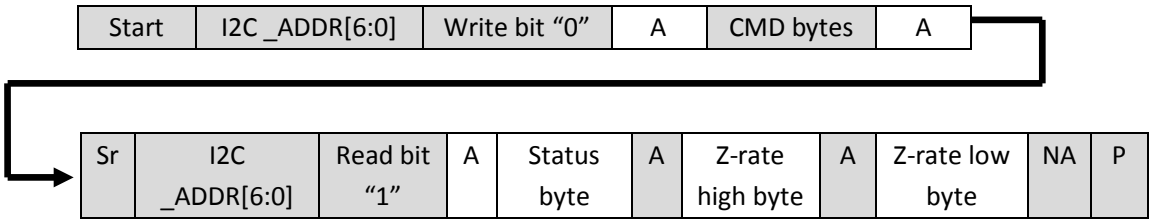
1.1.12.1 Example of command usage

Start	I2C _ADDR[6:0]	Write bit “0”	A	CMD1 byte	A	CMD bytes(1)

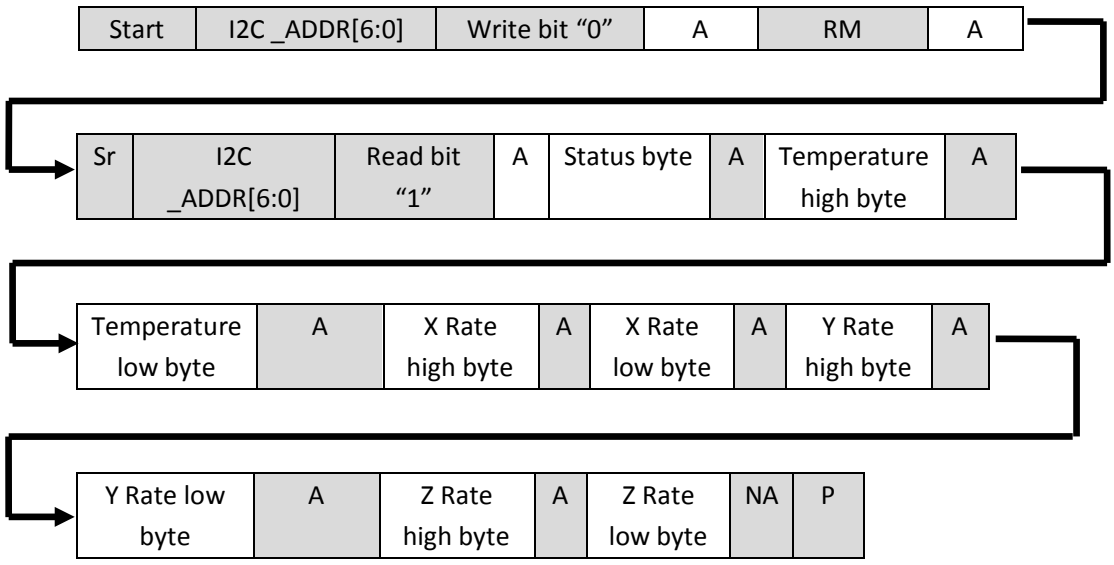


1.1.12.2 Read measurement RM

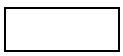
The command read measurement can get the sensor rate while the dc213 set out a int signal, generally speaking, the amounts of input bytes depends on the argument of <zyxt> in mode command, each bit represent two bytes of rate data, the RATA data order is fixed as temperature rate, rateX, rateY, rateZ. If we want’s rateZ only, the sequence of I2C should follow the rule:



If we want to acquire all of the data, the sequence of I2C should be organized as bellow:



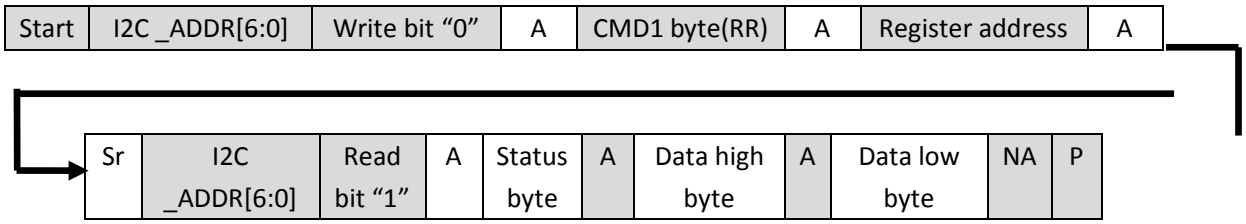
From dc213 to master



From master to dc213

1.1.12.3 Read Register(RR)

The volatile memory data can be read out by the command of read register (RR). The command byte should be followed while the I2C writing address has been sent out. Before a restart of I2C protocol, the register address needed, then the register data will be received following a read I2C address.



From dc213 to master

From master to dc213

1.1.12.4 Other commands

The usage of left commands is quite easy for they do not have input or output bytes, just follow the sequence bellow completely.

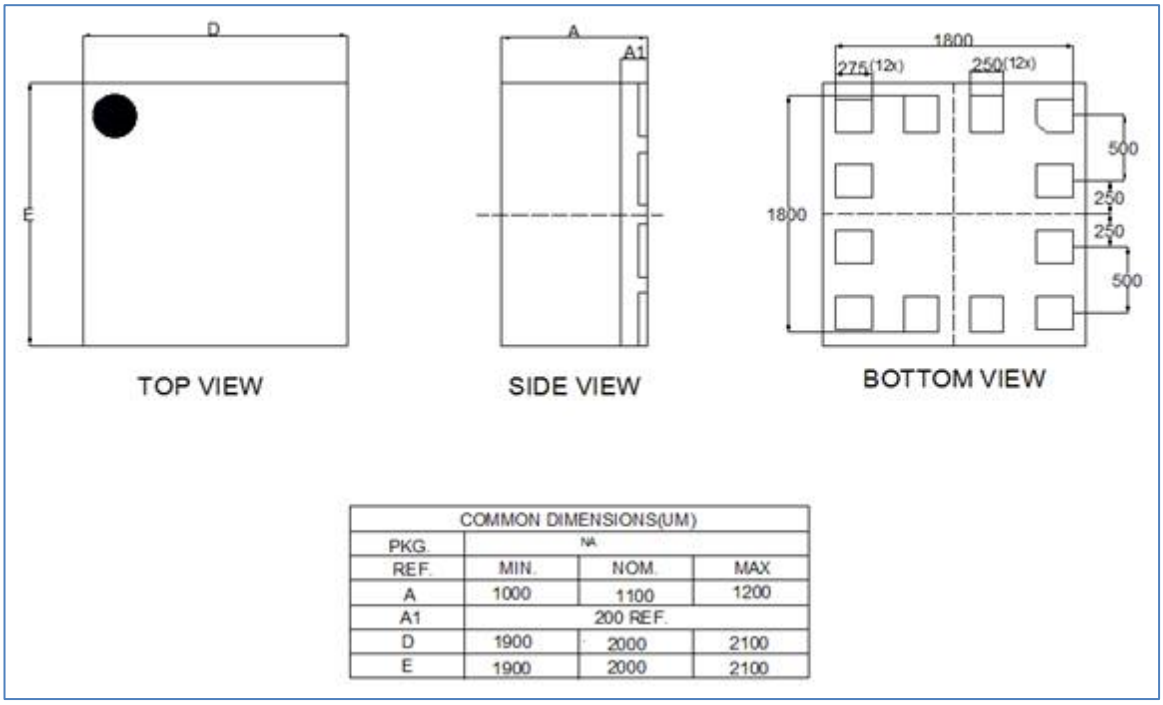
Start	I2C _ADDR[6:0]	Write bit "0"	A	CMD1 byte	A	Sr	I2C _ADDR[6:0]	Read bit "1"	A	Status byte	NA	P

From dc213 to master

From master to dc213

10 Package information

Outline dimensions



COMMON DIMENSIONS(UM)			
PKG.	NA		
REF.	MIN.	NOM.	MAX.
A	1000	1100	1200
A1		200 REF.	
D	1900	2000	2100
E	1900	2000	2100

Figure 12 12 Pin LGA Mechanical data and package dimensions

Tape and reel specification

The dc213 is shipped in a standard pizza box
The box dimension for 1 reel is: L x W x H = 35cm x 35cm x 5cm
dc213 quantity: 5000pcs per reel, please handle with care.

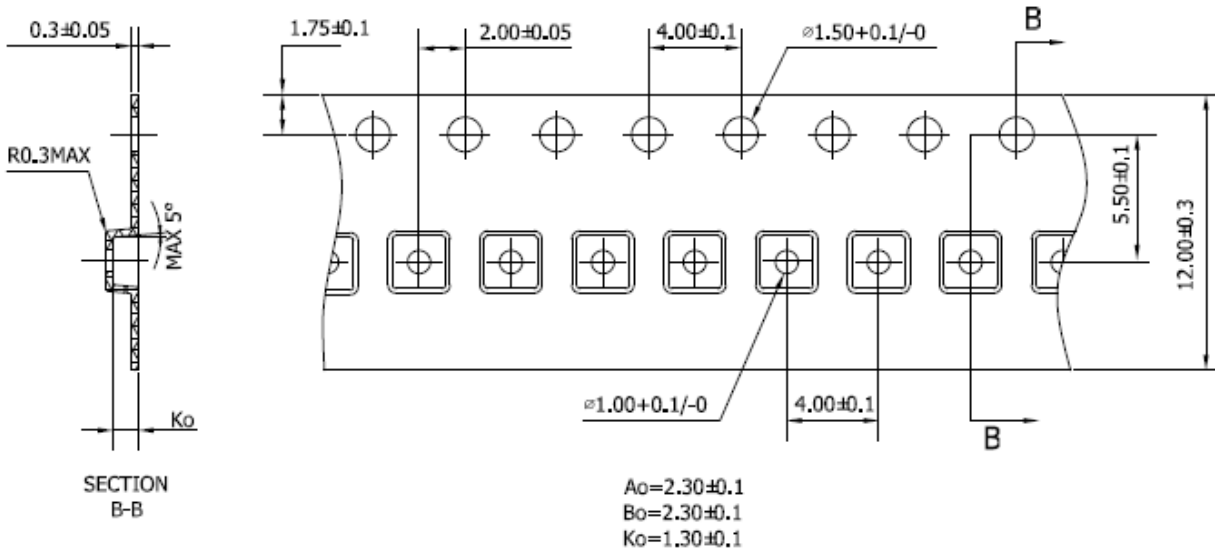


Figure 13 Tape and reel dimension in mm

11 Revision history

Table 96.Document revision history

Date	Revision	Changes
06-Aug-2014	0.1	Initial release
25-Sep-2014	0.2	Update Application hints
19-Dec.-2014	0.3	Modify the package outline dimensions